# CAS-1000-I2C/E



Bus Analyzer, Exerciser, Emulator, and Programmer

While the I<sup>2</sup>C interface seems simple on the surface, this straightforward architecture is not immune to intermittent glitches, device misbehaviors, and protocol violations. Likewise, tracking down these errors can be tedious business if the right tool is not utilized. The CAS-1000-I2C/E bus analyzer is an exceptional tool for pinpointing I2c irregularities. The ability to spot complex problems and identify invisible obstacles make it the preferred I<sup>2</sup>C development solution. Advanced logging, debugging, emulation, and verification capabilities offer power and versatility, yet the Windows-based user interface makes the most complex features simple to use.

The CAS-1000-I2C/E succeeds where simple monitoring and interactive I/O tools fall short—a complete solution to monitoring, emulating, stressing, and characterizing I<sup>2</sup>C and SMBus interfaces.



# Features

- Supports I2C and SMBus monitoring and traffic generation for Standardmode, Fastmode, Fast-mode Plus (Fm+) with I2C bus data rates up to 5 Mbit/s
- Monitors and emulates simultaneously —up to 1 emulated master and 10 emulated slaves, all running concurrently with high-speed mode (Hs-mode) monitoring
- Measures I2C bus electrical & timing parameters with a graphical waveform display
- Injects glitch & signal patterns, protocol errors, & slave clock stretching to override the bus and stress the UUT
- Adjustable bus voltage reference and software, configurable pull-up resistors on the SDA and SCL lines
- Powerful command and script language for emulation control and automated testing
- Passive traffic monitoring with state and timing recording, time stamping, message filtering, and symbolic translating
- Unlimited and continuous logging of transaction data to file
- Captures advanced trigger events to highlight and display bus transactions of interest
- In-System Programming of I2C serial EEPROMs
- 32- and 64-bit APIs for integration with third party languages, including Python and LabVIEW
- High-speed, bus-powered USB 2.0 interface with I2C Exerciser software for Microsoft Windows

# Software

The CAS-1000-I2C/E is an advanced, feature-packed and powerful I2C debugging and analysis system. By providing full visibility as well as detailed control of the I2C bus, the CAS-1000-I2C/E enables engineers to save time and resources, replacing multiple instruments with a single intuitive and specialized tool. The Corelis hardware and software provide a convenient easy to use environment for hardware debugging, software development, bus validation, and in-system programming.

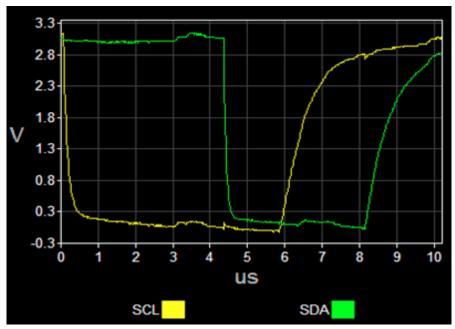
# **I2C Monitor**

Passively listens and records all I2C bus traffic while displaying captured data in real time in both state and waveform timing windows. Virtually unlimited trace data recording capability. Includes message filtering, symbolic translation, and event triggering. Bus signal and protocol conformance are continually evaluated with deviations flagged. The monitor window is shown below.

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	33		Data	Target	EEPROM	7-Bit	Read	NAK		102	1	1	12	2,929
	34	1	Address	Analyzer	ADC	7-Bit	Write			102	1	1		3,033
01101 	35		Data	Target	ADC	7-Bit	Write			102	1	1	40	3,128
altaltul	36 Cu	rsor A	Data	Target	ADC	7-Bit	Write			102	1	1	DONE	3,221
Monitor	37	1	Address	Analyzer	SLAVE_GPIO	7-Bit	Write			102	1	1		3,333
	38 Tri	gger	Data	Target	SLAVE_GPIO	7-Bit	Write			102		1	SLAVE_I01_LOW	3,427
<u></u>	39	1	Address	Analyzer	SLAVE_GPIO	7-Bit	Write			102	0	1		3,539
10	40 Cur	rsor B	Data	Target	SLAVE_GPIO	7-Bit	Write			102	0		SLAVE_I02_LOW	3,634
	41	1	Address	Analyzer	EEPROM	7-Bit	Read			102	0	0		3,746
Debugger	42		Data	Target	EEPROM	7-Bit	Read			102	0	0	3D	3,844
	43		Data	Target	EEPROM	7-Bit	Read			102	0	0	63	3,933
	44		Data	Target	EEPROM	7-Bit	Read			102	0	0	52	4,021
0110100 1001001	45		Data	Target	EEPROM	7-Bit	Read	NAK		102	0	0	16	4,110
Programmer	<													>
	Scale:	50 us/div	v -	+ Auto	Fit Line:	37	•	Interva	al A to B:		426	374 us		
39455	Scale:	50 us/div					> ( ,	Interva		,   ,	426	374 us		
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I2C Exerciser Monitor: Log, analyze, and display trace and timing data.

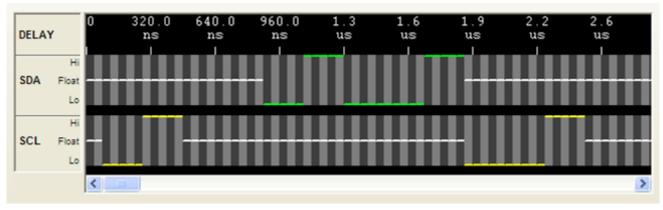
The CAS-1000-I2C/E leaves standard serial bus analyzers behind by providing a complete, peerless set of tools to generate bus traffic, inject glitches and protocol errors, measure bus electrical and timing parameters, program serial EEPROMs, emulate I2C masters and slaves, and more—all while simultaneously monitoring the bus, logging trace and timing data, and verifying I2C bus behavior on the fly. The I2C Exerciser software interface, included with the CAS-1000-I2C/E, provides a consolidated and intuitive GUI (Graphical User Interface) for host PC control and visualization of all bus monitoring and traffic generation features.



Parameters Scope: Measure and display common I2C Bus electrical and timing parameters.

## **I2C Parameters Scope**

Using the Parameters Scope tool, the CAS-1000-I2C/E can be utilized to quickly measure and return the basic electrical and I2C timing parameters of the target bus without setting up the advanced scripting functions of the Test tool. It can gather master specific and slave-specific parameters, such as signal timing characteristics, and also system-wide parameters, such as bus voltage, pull-up resistance, and capacitance. Each measurement is compared to maximum and minimum values loaded from a specification file and the resulting pass or fail status is shown with the measurement. The Parameters Scope provides the additional ability to display a graph of captured signal edge transition data and a trigger can be set to capture a particular I2C bus signal's rising or falling edge.



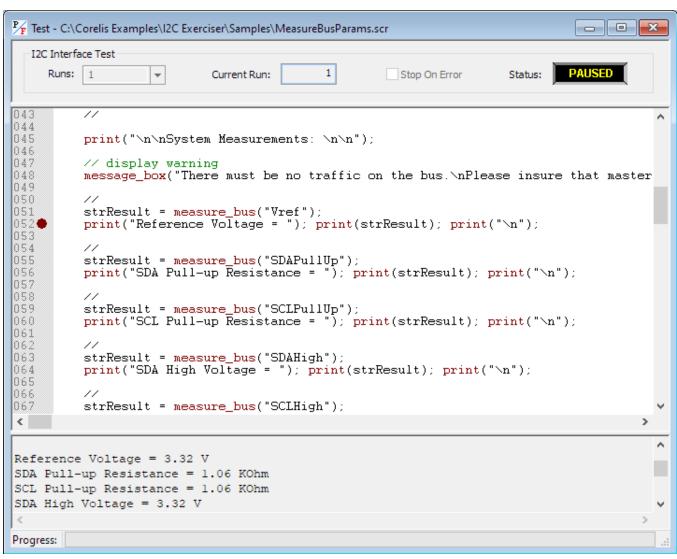
Glitch Pattern Editor: Create and inject customized digital patterns to stress I2C buses.

# **I2C Emulator**

Enables concurrent virtual devices programmed to interact with the bus in addition to those of the target. These can include a Master (capable of multi-master arbitration), and up to 10 slaves. The above monitor includes and tags this emulated traffic.

#### **I2C Tester**

Interprets a script program file to control a go-no-go test sequence, including bus electrical/timing parametric measurements. This enables automatic target bus specification compliance and functionality validation. It is suitable for design/development as well as factory acceptance testing. The test script window is shown below.





# **I2C Debugger**

A user interactive bus I/O access portal. This enables individual bus transfers for immediate target communications. Looping supports repeated I/O patterns to facilitate external signal observations. Besides generic writing and reading of data blocks, a growing library of known standard devices is included showing interactive screens tailored to the device's organization (such as ADCs, DACs, flash memories, SMbus behavior, etc.). The debugger window is shown below.

Send	Receive
Addr: C4  AddrType: 7-Bit	Addr: 18  AddrType: 7-Bit
Run: Single -	Bytes: 1
No Stop	No Stop
<pre>// ADDRESS_MODE: FE // tutorial script address 2A 33 pause 500 // milliseconds address 18 FF 00 pause 500 address C4 21 30 0D 0A</pre>	33 FF 00 21 30 0D 0A
<	

# **I2C Programmer**

Provides easy-to-use high-speed in-system programming of I2C compatible serial EEPROMs. Two programmer windows are shown below.

Programmer - C:\Corelis I	Examples\Boards\24xx512.pcf
Device Selection	
Manufacturer:	Generic I2C EEPROM ▼
Type:	24xx00 (16 Byte I2C EEPROM)
I2C Device Address:	A0 ▼ Address Type: 7-Bit ▼
Data File	
C:\Corelis Examples\E	Boards\Sequential256.exo <u>B</u> rowse
Offset: Add	▼ 0
<u>R</u> ead	Program Verify Erase

CAS-1000-I2CE Programmer Window

Address	Data														
0000000:	00 00	00	01	00	02	00	03	00	04	00	05	00	06	00	07
00000010:	00 08	00	09	00	0A	00	0B	00	0C	00	0D	00	0E	00	OF
00000020:	00 10	00	11	00	12	00	13	00	14	00	15	00	16	00	17
00000030:	00 18	00	19	00	1A	00	1B	00	1C	00	1D	00	1E	00	1F
00000040:	00 20	00	21	00	22	00	23	00	24	00	25	00	26	00	27
00000050:	00 28	00	29	00	2A	00	2B	00	2C	00	2D	00	2E	00	2F
00000060:	00 30	00	31	00	32	00	33	00	34	00	35	00	36	00	37
00000070:	00 38	00	39	00	3A	00	3B	00	3C	00	3D	00	3E	00	3F
00000080:	00 40	00	41	00	42	00	43	00	44	00	45	00	46	00	47
00000090:	00 48	00	49	00	4A	00	4B	00	4C	00	4D	00	4E	00	4 F
000000A0:	00 50	00	51	00	52	00	53	00	54	00	55	00	56	00	57
000000B0:	00 58	00	59	00	5A	00	5B	00	5C	00	5D	00	5E	00	5F
000000C0:	00 60	00	61	00	62	00	63	00	64	00	65	00	66	00	67
000000D0:	00 68	00	69	00	6A	00	6B	00	6C	00	6D	00	6E	00	6F
000000E0:	00 70	00	71	00	72	00	73	00	74	00	75	00	76	00	77
000000F0:	00 78	00	79	00	7A	00	7B	00	7C	00	7D	00	7E	00	7F
Address															

CAS-1000-I2CE Programmer Read Device Contents Window

One application of the CAS-1000-I2C/E is to rapidly validate compliance of a target bus with the specification. This is supported at the electrical, timing, as well as the signaling level. Another application is to passively monitor any I/O activity transpiring on a target bus. This includes the detection of errant protocol. All such logged information is time stamped for history reconstruction. A third application is the programmed interchange of messages with the target bus system, also recorded by the monitoring function. This method can serve to generally exercise the target bus. It also supports target code development with debug stand-ins for non-existent bus devices. Finally, a general user PC to I2C communications link provides quick and direct visibility/control of target devices. This is extended to user applications via the provided API.

The System Management Bus, or SMBus, was defined by Intel<sup>®</sup> Corporation in 1995 and is based on the I2C bus architecture. It is used in personal computers and servers for low-speed system management communications.

SMBus is a two-wire interface through which simple system and power management related chips can communicate with the rest of the system. A system using SMBus as a control bus for these system and power management related tasks passes messages to and from devices by addressed transfers, enabling moderate transfer rates using minimal board resources. With System Management Bus, for example, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspend event, report different types of errors, accept control parameters, and return its status. The SMBus may share the same host device and physical bus with standard I2C components. Intel originally conceived the SMBus as the communication bus to accommodate Smart Batteries and other system and power management components.

The CAS-1000-I2C/E software features SMBus decoding for common SMBus devices. Ordinarily, the raw data of the I2C transactions between SMBus devices must be manually decoded into meaningful information. With the SMBus decoding feature, a specific device address can be associated with a text file containing decoding information which allows the I2C Exerciser software to do the interpretation automatically.

🔀 I2C Exerciser - Untitled\* - [Monitor - (Untitled)\*] Eile Trace Tools Window Help 5 📔 😂 🖶 🕨 📩 II 🕺 🖅 🖅 💷 🕮 💷 💷 🕼 😭 🔛 🥹 Shortcuts Line Marker NAK Error KHz | 1/0 1 1/0 2 Туре Location Addr (Hex) AddrType R/W Data Byte (SMBus) Time (us) 12 Addre Target ADC 7-Bit Write 400 1.522 SMBus A. 7-Bit 17 Target 402 1,843 Addre Re. Monito 18 SMBus A. 402 Data 7-Bit DEVICE=1A 0x7 1,884 Analyzer Re.. 35 Analyzer ADC 7-Bit 107 2,476 Addre. Re. 36 Data ADC 7-Bit Re. 104 1CDONE 2,632 Target 17 38 Addre Target 54 7-Bit Write 402 3,441 39 Data Target 54 7-Bit Write 402 17 5D 35 0F 3,469 43 Addre Analyzei 36 7-Bit Re. 107 3,729 44 46 Addre Target SMBus A. 7-Bit Re 402 4 6 9 4 1 402 47 Data Analyzer SMBus A 7-Bit Re. DEVICE=3C 0x6 4.735 51 Addre. Analyzer ADC 7-Bit 107 4.995 Re.. Target Re. 52 Data ADC 7-Bit 104 1FBUSY 5.151 54 Addre. Target PLL 7-Bit Write 402 5.960 55 Data Target PLL 7-Bit Write 402 5A 5.988 56 Addre. Target ADC 7-Bit Write 401 6.171 1 57 Tagged Data Target ADC 7-Bit Write 403 33 E7CHANSEL 6,199 62 7-Bit Addre Target 54 Write 402 6,546 50 us/div + Auto Fit 44 • • 9.422762 ms Scale: Interval A to B: Line: FIELD 01010100A 00001101A S0011011RA K SDA M wwwww Þſ DEMO AddrFormat: FE Trace Off SCL: -Bus: -SDA: -1/0 1: -1/0 2: -

The CAS-1000-I2C/E also supports SMBus PEC (Packet Error Checking) message generation.

CAS-1000-I2CE Bus Monitor Window in SMBus Decoding Mode

## Hardware

At the core of the CAS-1000-I2C/E is an on-board engine whose logic performs the low level interaction with the I2C bus. This element receives set-up, direction and drive data from the host via a USB 2.0 port. Conversely, as bus activity is detected and characterized, its transitional information is conveyed up to the host for further processing.

The PC host operates this processor via the USB 2.0 port under the provided Windows application. Alternatively, the user may create custom software which calls included API C/C++ library routines to easily operate the I2C I/O, avoiding hardware management details.

In addition there is an array of onboard physical interface elements to facilitate the required measurement, capture, and operating capabilities. This includes a number of DACs to develop the various programmable voltages.

High-speed A2D converters enable the capture of I2C bus waveforms for analysis, including sensing adjustable thresholds (with hysteresis), signal level crossing detection, and transition time determination.

## **Programmable Clock Rate**

The CAS-1000-I2C/E clock rate is programmable under software for use when emulating a master. It is capable of supporting standard mode and fast mode transfers of up to 5 Mbits/sec as well as intermediate values. For emulated slaves, clocking comes from the target, whose rate is automatically accommodated up to 5 MHz since the clock rate automatically tracks the target bus master.

# Test Discrete I/O Signals

Two programmable lines can be operated under PC host software control. They are available to stimulate the target system or sense target conditions in coordination with the testing. Each line is programmable as input, output, or output open-drain. One of these outputs can be a dedicated trigger and programmably linked to the SMB output trigger connector for test synchronization with external laboratory equipment. The other discrete I/O can be tied to the other SMB connector as an input trigger.

# **Adjustable Voltage Levels**

The signal level of the set of discrete I/O and trigger lines is programmable from 1.25V to 3.3V in increments of 50mV. The I2C bus reference voltage can be programmed as target driven through its bus pull-ups or driven from the CAS-1000-I2C/E I2C analyzer. This target reference voltage can also be measured. When the CAS-1000-I2C/E is programmed to source this reference level (both SCL and SDA signals), the voltage can be set with 100mV resolution over the range of 0.8V to 5V. When the CAS-1000-I2C/E reference voltage drives the bus, one of a set of pull-up resistors can be selected. The resistor values span the range from 250 to 50K ohms. Additionally, sensed bus signal high and low individual threshold levels can be adjusted. This supports the bus hysteresis requirements. Default software-determined values are available.

# **Auxiliary TAP Port**

The CAS-1000-I2C/E includes an IEEE-1149.1 JTAG Test Access Port (TAP). This port can be used to perform boundary-scan testing and in-system programming of flash, EEPROMs and PLDs on the target system and is both hardware and software compatible with the complete ScanExpress<sup>™</sup> family of IEEE-1149.1 test and in-system programming products offered by Corelis. This feature is mutually exclusive to the I2C functionality and requires it to be put into the JTAG mode.

Configuration Manager	×
Filters Symbols SMBus Target Slaves Settings Files Timing Skew	1
Bus Electrical Features          Voltage Source       Bus Signal Thresholds         O Target Supplied       Image: Supplied	
Intended Pull-up Parameters Voltage: 3.30 ▼ Volts Low Level: 0.90 ▼ Volts	
Pull-up Resistance: 1000 V Ohms Auto Detect	
Bus Drive and Monitoring Features         Drive Clock Rate:       100 kHz         Accelerated Rising Edge Drive       Disable Collision Detection         Auto       On         On       Off	
Input/Output Signals	
High Level Function I/O 1: In    Drive SMB AT1	
I/O 2: In ▼ Source: Target ▼	
Monitor Buffer Options Depth: 64K ▼ Transactions □Log to File: C Exerciser\Trace.tdf	
Close	_

CAS-1000-I2CE Hardware Configuration Window

# Hardware Specifications

#### • General

Mechanical Dimensions	5.48 x 1.00 x 4.66 (+/- 0.25) inches
Shipping Weight	7 pounds (approximate)
Certifications	RoHS Compliant , CE Marked

#### • USB Interface

USB Transfer Rate	High-speed USB 2.0
USB Cable	Ships with a 6 foot USB 2.0 A to B cable

# • I2C Interface

I2C Bus Connector	RJ45 (AMP P/N 406549-1)
I2C Bus Cable	Ships with a 12 inch interface cable that termi-nates in flying lea ds suitable for connection to 0.025" square posts. Test clips are i ncluded.